ANNA UNIVERSITY, CHENNAI
AFFILIATED INSTITUTIONS
M. E. VLSI DESIGN AND EMBEDDED SYSTEMS
REGULATIONS – 2017
CHOICE BASED CREDIT SYSTEM

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs) :

I. To enrich students to excel in research leading to cutting edge technology in VLSI design and embedded systems and creating competent, innovative, and productive professionals in this field.
II. To provide students with a solid foundation in digital and computer architecture principles leading to VLSI design.
III. To understand the various applications and employ embedded systems to find solutions to them with good scientific and engineering knowledge so as to comprehend, analyze, design, and create novel products and solutions for the real life problems.
IV. To provide students with an academic environment aware of excellence, leadership, ethical conduct, positive attitude, societal responsibilities and the lifelong learning needed for a successful professional career.
V. To inculcate entrepreneurial skills in starting industries applying embedded system technologies.

PROGRAMME OUTCOMES (POs):

On successful completion of the programme,

1. Graduates will be able to apply the knowledge of computing, mathematics, science and electronic engineering for designing VLSI circuits.
2. Graduates will have an ability to identify, formulate, investigate and solve the issues related to the design of VLSI and embedded systems.
3. Graduates will have an ability to design and conduct experiments, perform analysis and interpret the problems of VLSI design and embedded systems.
4. Graduates will be able to demonstrate the design of an embedded system, component or process as per needs and specifications.
5. Graduates will demonstrate an ability to visualize and work on laboratory and multidisciplinary tasks.
6. Graduates will have the skills to use modern engineering tools, softwares and equipments to analyze problems.
7. Graduates will demonstrate knowledge of professional and ethical responsibilities.
8. Graduate will be able to communicate effectively in both verbal and written form.
9. Graduate will show the understanding of the impact of engineering solutions on the society and also will be aware of contemporary issues.
10. Graduate will develop confidence in self education and ability for lifelong learning.

Programme Educational Objectives	Programme Outcomes									
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**
I	✓	✓	✓	✓	✓	✓		✓	✓	✓
II		✓	✓		✓	✓				
III				✓	✓	✓	✓			
IV		✓	✓				✓	✓	✓	✓
V		✓	✓	✓				✓	✓	✓

YEAR	SEM	SUBJECTS	PROGRAM EDUCATIONAL OBJECTIVES									
			PE1	PE2	PE3	PE4	PE5	PE6	PE7	PE8	PE9	PE10
FIRST YEAR	I	Advanced Applied Mathematics	✓	✓			✓				✓	
		Digital Integrated Circuit Design		✓	✓	✓	✓	✓				
		Introduction to Embedded Controllers		✓		✓	✓	✓			✓	
		CMOS Analog IC Design		✓	✓		✓	✓				
		Advanced Digital System Design		✓	✓	✓	✓	✓	✓	✓		
		ASIC Design										
		Analog & Digital System Design Lab			✓	✓	✓	✓	✓	✓		✓
		FPGA System Design Lab										
	II	Real Time Embedded Systems		✓		✓	✓	✓			✓	
		VLSI Signal Processing		✓	✓	✓	✓	✓	✓		✓	✓
		Hardware-Software Co-design of Embedded system		✓	✓	✓	✓	✓	✓		✓	✓
		Low Power VLSI Design		✓	✓	✓	✓	✓			✓	✓
		Professional Elective-I										
		Professional Elective-II										
		Embedded Systems Lab			✓	✓	✓	✓	✓	✓		✓
		Technical Seminar and Report Writing										
SECOND YEAR	III	Professional Elective-III		✓	✓	✓	✓	✓	✓		✓	✓
		Professional Elective-IV										
		Professional Elective-V										
		Project Work Phase-I				✓		✓		✓		✓
	IV	Project Work Phase-II				✓		✓		✓		✓

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CHOICE BASED CREDIT SYSTEM
I – IV SEMESTER CURRICULA AND SYLLABI
SEMESTER - I

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	MA5167	Advanced Applied Mathematics	FC	4	4	0	0	4
2.	VE5101	Digital Integrated Circuit Design	PC	3	3	0	0	3
3.	VE5102	Introduction to Embedded Controllers	PC	3	3	0	0	3
4.	VE5103	CMOS Analog IC Design	PC	3	3	0	0	3
5.	AP5151	Advanced Digital System Design	PC	3	3	0	0	3
6.	VE5104	ASIC Design	PC	3	3	0	0	3
PRACTICALS								
7.	VE5111	Analog and Digital CMOS VLSI Design Laboratory	PC	4	0	0	4	2
8.	VE5112	FPGA System Design Laboratory	PC	4	0	0	4	2
			TOTAL	**27**	**19**	**0**	**8**	**23**

SEMESTER - II

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	CU5092	Real Time Embedded System	PC	3	3	0	0	3
2.	VL5291	VLSI Signal Processing	PC	3	3	0	0	3
3.	VE5201	Hardware Software Co Design of Embedded System	PC	3	3	0	0	3
4.	VL5202	Low Power VLSI Design	PC	3	3	0	0	3
5.		Professional Elective-I	PE	3	3	0	0	3
6.		Professional Elective-II	PE	3	3	0	0	3
PRACTICALS								
7.	VE5211	Embedded Systems Laboratory	PC	4	0	0	4	2
8.	VE5212	Technical Seminar and Report Writing	EEC	2	0	0	2	1
			TOTAL	**24**	**18**	**0**	**6**	**21**

III SEMESTER

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.		Professional Elective-III	PE	3	3	0	0	3
2.		Professional Elective-IV	PE	3	3	0	0	3
3.		Professional Elective-V	PE	3	3	0	0	3
PRACTICALS								
4.	VE5311	Project Work Phase – I	EEC	12	0	0	12	6
			TOTAL	**21**	**9**	**0**	**12**	**15**

IV SEMESTER

SL. No	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
PRACTICALS								
1.	VE5411	Project Work Phase – II	EEC	24	0	0	24	12
			TOTAL	**24**	**0**	**0**	**24**	**12**

TOTAL NO. OF CREDITS:71

FOUNDATION COURSES (FC)

SL. NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
PRACTICALS								
1.	MA5167	Advanced Applied Mathematics	FC	4	4	0	0	4
			TOTAL	**4**	**4**	**0**	**0**	**4**

PROFESSIONAL CORE (PC)

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	VE5102	Introduction to Embedded Controllers	PC	3	3	0	0	3
2.	VE5101	Digital Integrated Circuit Design	PC	3	3	0	0	3
3.	VE5103	CMOS Analog IC Design	PC	3	3	0	0	3
4.	AP5151	Advanced Digital System Design	PC	3	3	0	0	3
5.	VE5104	ASIC Design	PC	3	3	0	0	3
6.	CU5092	Real Time Embedded Systems	PC	3	3	0	0	3
7.	VL5291	VLSI Signal Processing	PC	3	3	0	0	3
8.	VE5201	Hardware - Software Co-design of Embedded system	PC	3	3	0	0	3
9.	VL5202	Low Power VLSI Design	PC	3	3	0	0	3
10.	VE5111	Analog and Digital CMOS VLSI Design Laboratory	PC	4	0	0	4	2
11.	VE5112	FPGA System Design Laboratory	PC	4	0	0	4	2
12.	VE5211	Embedded Systems Lab	PC	4	0	0	4	2

PROFESSIONAL ELECTIVES (PE)

ELECTIVE - I

SL. NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	VE5001	VLSI Architectures for System Design	PE	3	3	0	0	3
2.	VE5002	Parallel and Reconfigurable Architectures	PE	3	3	0	0	3
3.	VE5003	Advanced CMOS Analog IC Design	PE	3	3	0	0	3
4.	VE5004	Distributed Embedded Computing	PE	3	3	0	0	3
5.	VE5005	Computer Aided Design Automation	PE	3	3	0	0	3

ELECTIVE - II

SL. NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	VE5006	Digital Image and Video Processing	PE	3	3	0	0	3
2.	VE5007	Algorithm for VLSI Design Automation	PE	3	3	0	0	3
3.	VE5008	Advanced Embedded System Design	PE	3	3	0	0	3
4.	VE5009	Power Management and Clock Distribution Circuits	PE	3	3	0	0	3
5.	VE5010	Adaptive Signal Processing	PE	3	3	0	0	3

ELECTIVE - III

SL. NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	VE5011	Digital Signal Processors and Architectures	PE	3	3	0	0	3
2.	CU5073	VLSI For Wireless Communication	PE	3	3	0	0	3
3.	VE5012	Computational Intelligence	PE	3	3	0	0	3
4.	VE5013	Embedded C	PE	3	3	0	0	3
5.	VE5014	Design of Embedded Control System	PE	3	3	0	0	3

ELECTIVE - IV

SL. NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	VL5002	RF IC Design	PE	3	3	0	0	3
2.	VE5015	MEMS and Microsystems	PE	3	3	0	0	3
3.	VE5016	Multi Core Architectures and Programming	PE	3	3	0	0	3
4.	VE5017	Embedded Automotive Systyems	PE	3	3	0	0	3
5.	VE5018	SoC Design for Embedded System	PE	3	3	0	0	3

ELECTIVE - V

SL. NO.	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	VL5005	Networks on Chip	PE	3	3	0	0	3
2.	AP5071	Nano Electronics	PE	3	3	0	0	3
3.	VL5009	Design and Analysis of Computer Algorithms	PE	3	3	0	0	3
4.	AP5093	Robotics	PE	3	3	0	0	3
5.	VE5019	Embedded Networking	PE	3	3	0	0	3

EMPLOYABILITY ENHANCEMENT COURSES (EEC)

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	VE5212	Technical Seminar and Report Writing	EEC	2	0	0	2	1
2.	VE5311	Project Work Phase –I	EEC	12	0	0	12	6
3.	VE5411	Project Work Phase –II	EEC	24	0	0	24	12

MA5167 ADVANCED APPLIED MATHEMATICS L T P C
4 0 0 4

OBJECTIVES:

- To encourage students to develop a working knowledge of the central ideas of linear algebra;
- To study and understand the concepts of probability and random variable of the various functions;
- To understand the notion of a Markov chain, and how simple ideas of conditional probability and matrices can be used to give a thorough and effective account of discrete-time Markov chains;
- To formulate and construct a mathematical model for a linear programming problem in real life situation;
- To introduce the Fourier Transform as an extension of Fourier techniques on periodic functions and to solve partial differential equations.

UNIT I LINEAR ALGEBRA 12

Vector spaces – norms – Inner Products – Eigenvalues using QR transformations – QR factorization - generalized eigenvectors – Canonical forms – singular value decomposition and applications – pseudo inverse – least square approximations --Toeplitz matrices and some applications.

UNIT II ONE DIMENSIONAL RANDOM VARIABLES 12

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT III RANDOM PROCESSES 12

Classification – Auto correlation - Cross correlation - Stationary random process – Markov process –- Markov chain - Poisson process – Gaussian process.

UNIT IV LINEAR PROGRAMMING 12

Formulation – Graphical solution – Simplex method – Two phase method - Transportation and Assignment Models.

UNIT V FOURIER TRANSFORM FOR PARTIAL DIFFERENTIAL EQUATIONS 12

Fourier transforms: Definitions, properties-Transform of elementary functions, Dirac Delta functions – Convolution theorem – Parseval's identity – Solutions to partial differential equations: Heat equations, Wave equations, Laplace and Poison's equations.

TOTAL :60 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Classify the random process.

CO2: Formulate and develop a mathematical model for linear programming problem

CO3: Apply the concept of fourier transform to real life situation

REFERENCES:

1. Bronson, R.Matrix Operation, Schaum's outline series, McGraw Hill, New york (1989).
2. Oliver C. Ibe, "Fundamentals of Applied Probability and Random Processes, Academic Press, (An imprint of Elsevier), 2010.
3. Taha H.A. "Operations Research : An introduction" Ninth Edition, Pearson Education, Asia, New Delhi 2012.
4. Sankara Rao, K. "Introduction to partial differential equations" Prentice Hall of India, pvt, Ltd, New Delhi, 1997.
5. Andrews,L.C. and Philips.R.L. "Mathematical Techniques for engineering and scientists", Printice Hall of India, 2006.
6. O'Neil P.V. "Advanced Engineering Mathematics", (Thomson Asia pvt ltd, Singapore) 2007, cengage learning India private limited.

VE5101	DIGITAL INTEGRATED CIRCUIT DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To study and realize various building blocks of digital VLSI circuits in transistor level.
- To design the architectural choices and performance tradeoffs involved and to realize circuits in CMOS technology.
- To introduce the design knowledge about CMOS testing and its implementation strategies.

UNIT I MOS TRANSISTOR PRINCIPLES 9

MOS Technology and VLSI, Pass transistors, NMOS, CMOS Fabrication process and Electrical properties of CMOS circuits and Device modeling, Characteristics of CMOS inverter, Scaling principles and fundamental limits. Propagation Delays, CMOS inverter scaling, Stick diagram, Layout diagram, Layout rules, Elmore's constant, Logical Effort.

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Static CMOS logic Design, Design techniques to improve the speed, power dissipation of CMOS logic, low power design techniques, Ratioed logic, Pass transistor Logic, Transmission gate logic, CPL, DCVSL, Dynamic CMOS logic, Domino logic, Dual Rail logic, NP CMOS logic and NOR array logic.

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static and Dynamic Latches and Registers, Timing Issues, Pipelines, Clocking strategies, Clock Domain Crossing - Analysis, Strategies and Implementation - Memory Architectures, and Memory control circuits.

UNIT IV DESIGNING ARITHMETIC BUILDING BLOCKS 9

Datapath circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area tradeoffs.

UNIT V CMOS TESTING AND IMPLEMENTATION STRATEGIES 9

Need for testing -Manufacturing test – Design for testability – Boundary scan, Full Custom and Semicustom Design, FPGA building block architectures, FPGA interconnects.

TOTAL:45 PERIODS

COURSE OUTCOMES:

After completion of this course:

- Ability to expand their knowledge in designing circuit level implementation to realize and test system based architectures, which include digital, memory, and mixed-signal subsystems.

REFERENCES:

1. Jan Rabaey, Anantha Chandrakasan, B.Nikolic, "Digital Integrated Circuits: A Design Perspective", Prentice Hall of India, 2nd Edition, 2003.
2. N.Weste, K.Eshraghian, "Principles of CMOS VLSI Design", A System Perspective, Addision Wesley, 2nd Edition, 1993.
3. A.Pucknell, Kamran Eshraghian, "Basic VLSI Design", Prentice Hall of India, 3rd edition, 2007.
4. John. F. Wakerly "Digital Design :Principles and Practices", Pearson, 5th Edition 2018.
5. M.J. Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997.
6. R.Jacob Baker, Harry W.LI., David E.Boyee, "CMOS Circuit Design, Layout and Simulation", 2005, Prentice Hall of India.

VE5102 INTRODUCTION TO EMBEDDED CONTROLLERS L T P C
3 0 0 3

OBJECTIVES:

- To learn about the designing of an embedded system for commercial applications.
- To learn the features, architecture and programming of PIC and ARM microcontrollers
- To study the interfacing peripherals with microcontrollers.
- To learn about the communication protocols in a Microcomputer system.
- To learn about the fundamentals of real-time operating system in an embedded system.

UNIT I INTRODUCTION TO EMBEDDED SYSTEMS 9

Processor Embedded into a System, Embedded Hardware Units and Devices in a System, Embedded Software in a System, Examples of Embedded Systems, Embeded System on-chip (Soc) and Use of VLSI Circuit Design Technology, Complex Systems Design and Processors, Design Process in Embedded Systems, Formalization of System Design, Design Process and Design Examples, Classification of Embedded Systems.

UNIT II ATMEGA MICROCONTROLLERS 9

Architecture, Features, Memory and memory map, I/O ports, Timers and CCP Devices, ADC, Interrupts, Instruction format, Addressing Modes, Instruction Set, Programming with MPLAB IDE.

UNIT III 16 BIT MICROCONTROLLER 9

Introduction to 16 bit Processors, MSP430 - RISC CPU Architecture - Compiler friendly features - Instruction sets - Clock System - Memory Subsystem - Bus Architecture, different families in MSP 430 (2xx,4xx,5xx,6xx) - Key differentiating factors between families.

UNIT IV INTERFACING I/O DEVICES AND COMMUNICATION PROTOCOLS 9

LED, liquid crystal display, Motor (DC, Servo, Stepper), Relays, Keypad, Keyboard, Touch screen, Sensors (thermocouple, force, displacement), SD card, Infrared connectivity, Serial communication protocols (UART, I2C, SPI, CAN, USB, LIN), Parallel communication protocols (PCI, ISA), Wireless communication networks (Bluetooth, Xbee, Wifi, GSM), Global positioning system receivers, Embedded Systems and the internet.

UNIT V MULTITASKING AND THE REAL-TIME OPERATING SYSTEM 9

The challenges of multitasking and real-time, Achieving multitasking with sequential programming, RTOS, Scheduling and the scheduler, Developing tasks, Data and resource protection- the semaphore,Examples using Salvo Real-time operating systems.

TOTAL:45 PERIODS

OUTCOMES:

After completion of this course:

- Students will be able to interface peripherals with microcontrollers.
- Students will be able to design an embedded system in real time.
- Students will be able to use the communication protocols in application specific.

REFERENCES:

1. Raj Kamal, "Embedded Systems- Architecture, Programming and Design", Tata Mc Graw-Hill Publications, 2nd Edition, 2008.
2. John Davies, "MSP 430 Microcontroller Basics", Elsevier, 2008.
3. Yifeng Zhu,"Embedded Systems with ARM Cortex-M3 Microcontrollers in Assembly Language and C**",** E-Man Press LLC, 1st Edition, 2014.
4. Tim Wilmshurst, "Designing Embedded Systems with PIC Microcontrollers-Principles and Applications", Newnes Publications, 2007.
5. Julio Sanchez Maria P.Canton, "Microcontroller Programming: The microchip PIC", CRC Press, Taylor & Francis Group,2007.
6. Thomas Grace, **"**Programming and Interfacing Atmel AVR Microcontrollers", Cengage Learning PTR, 2015.

VE5103 **CMOS ANALOG IC DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- The course will discuss the equivalent circuits and models of MOS circuits.
- To analyze bias circuits using CMOS current mirrors.
- To design and analyze the frequency response of multistage differential amplifiers.
- To discuss the stability and frequency compensation of feedback amplifiers.

UNIT I SINGLE STAGE AMPLIFIERS 9

Review of MOS physics and equivalent circuits and models. Large and Small signal analysis CS, CG and source follower, miller effect, frequency response of CS, CG and source follower.

UNIT II CURRENT MIRRORS 6

Current Sources, Basic Current Mirrors, Cascode stages for Current mirrors , Wilson Current Mirror, Large and small signal analysis of current mirrors.

UNIT III MULTISTAGE DIFFERENTIAL AMPLIFIERS 12

Differential amplifier, Large and small signal analysis of the balanced differential amplifier, device mismatches in differential amplifier, small and large signal analysis of the differential pair with current mirror load, $PSRR^+$, $PSRR^-$ and CMRR of differential amplifiers, small signal analysis of telescopic amplifier, two-stage amplifier and folded cascaded amplifier.

UNIT IV FREQUENCY RESPONSE OF MULTISTAGE DIFFERENTIAL AMPLIFIERS 9

Dominant-Pole approximation, zero-value time constant analysis, - Frequency response of current mirror loaded, differential amplifier, short circuit time constants, frequency response of telescopic cascaded, folded cascode amplifier.

UNIT V STABILITY AND FREQUENCY COMPENSATION OF FEEDBACK AMPLIFIERS 9

Properties and types of negative feedback circuits, feedback configurations, effect of loading in feedback networks, feedback circuit analysis using return ratio- modelling input and output port in feedback network, the relation between gain and bandwidth in feedback amplifiers, phase margin, frequency compensation, compensation of two stage MOS amplifiers.

TOTAL:45 PERIODS

COURSE OUTCOMES:

After completion of this course, students are expected to:

- Be able to analyze and design CMOS analog IC building blocks like MOS amplifiers, current mirrors and multistage differential amplifiers.

REFERENCES:

1. Gray, Hurst, Lewis, Meyar, “Analysis and Design of Analog Integrated Circuits” John Wiley, 5th Edition, 2009.
2. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Twelfth Reprint, Tata Mc Graw Hill, 2012.
3. Phillip E. Allen, Douglas R.Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 3rd Edition, 2011.
4. Jacob Baker “CMOS: Circuit Design, Layout, and Simulation”, Wiley IEEE Press, 3rd Edition, 2010.

AP5151 ADVANCED DIGITAL SYSTEM DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To introduce methods to analyze and design synchronous and asynchronous sequential circuits.
- To introduce the architectures of programmable devices.
- To introduce design and implementation of digital circuits using programming tools.

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-ASM chart and realization using ASM

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

UNIT V SYSTEM DESIGN USING VERILOG 9

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

At the end of the course, the student should be able to:

- Analyze and design sequential digital circuits
- Identify the requirements and specifications of the system required for a given application
- Design and use programming tools for implementing digital circuits of industry standards

REFERENCES:

1. Charles H.Roth Jr “Fundamentals of Logic Design”, Thomson Learning, 2004.
2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999.
3. M.G.Arnold, “Verilog Digital – Computer Design”, Prentice Hall (PTR), 1999.
4. Nripendra N Biswas “Logic Design Theory”, Prentice Hall of India,2001.
5. Parag K.Lala “Digital system Design using PLD”, B S Publications, 2003.
6. Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design”, B S Publications,2002.
7. S. Palnitkar , “Verilog HDL – A Guide to Digital Design and Synthesis”, Pearson , 2003.

VE5104 **ASIC DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- To study the basic concepts of digital CMOS Application Specific Integrated Circuit (ASIC) systems design and library cell design.
- To know the architectural details of programmable ASICs.
- To present the ASIC physical design flow, including logic synthesis, floor-planning, placement and routing.
- To know back-end physical design flow steps through VLSI CAD tools.

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors – Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 – Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING 9

System partitioning - partitioning methods - floor planning - placement - physical design flow – Routing - global routing - detailed routing - special routing - circuit extraction -DRC.

TOTAL:45 PERIODS

COURSE OUTCOMES:

Upon completion of this course, the students will:

- Be able to design the ASIC implementation using programmable ASIC devices.
- Be able to comprehend the different issues related to the development of ASIC designs including logic synthesis, floor-planning, placement and routing, tools and future trends.

REFERENCES:

1. M.J.S .Smith, "Application Specific Integrated Circuits", Addison - Wesley Longman Inc., 1997, Reprint 2004.
2. Farzad Nekoogar and Faranak Nekoogar, "From ASICs to SOCs: A Practical Approach", Prentice Hall PTR, 2003.
3. Wayne Wolf, "FPGA-Based System Design", Prentice Hall PTR, 2004.
4. R. Rajsuman, "System-on-a-Chip Design and Test. Santa Clara, CA: Artech", House Publishers, 2000
5. F. Nekoogar. "Timing Verification of Application-Specific Integrated Circuits (ASICs)", Prentice Hall PTR, 1999.

VE5111 ANALOG AND DIGITAL CMOS VLSI DESIGN LABORATORY L T P C
0 0 4 2

OBJECTIVES:

- To understand the various analog and digital circuits and their simulation using Cadence tool.
- To learn the advanced concepts of modern VLSI circuit and system design
- To design common sequential functions: flip-flops, registers, latches, and state-machines.
- To understand placement, routing, and verify timing of a standard cell design.

DIGITAL DESIGN (HDL Design Entry Tool):

1. HDL based design entry and simulation of Parameterizable cores of Counters, Shift registers, State machines, 8-bit Parallel adders and 8 –Bit multipliers.
2. HDL based design entry and simulation of Parameterizable cores on the simple Distributed Arithmetic system.
3. HDL based design entry and simulation of Parameterizable cores on memory design and 4 – bit ALU.
4. Synthesis, P&R and post P&R simulation, Critical paths and static timing analysis results to be identified.

ANALOG IC DESIGN (USING SPICE CIRCUIT SIMULATION TOOL):

Circuit simulation, Layout generation, parasitic extraction, Synthesis and Standard cell based design of the circuits. Identification of critical paths, power consumption. P&R, power and clock routing, post P&R simulation and Static timing analysis of:

1. Design of CMOS Inverter - Circuit Simulation, transfer characteristic curve, transient analysis, Layout design.
2. Design of Current Mirrors - Simple current source generator, Current mirror, Wilson Current mirror circuit, Layout of the current mirror circuit.
3. A simple differential amplifier. Measure gain, ICMR, and CMRR - Differential input, single ended differential amplifier design, Differential amplifier design, telescopic amplifier design, layout of differential amplifier.

TOTAL : 60 PERIODS

COURSE OUTCOMES:

After the completion of this lab, Students should be able:

- To create the hierarchical decomposition of sequential designs.
- To perform synthesis and analysis of combinational and sequential designs.

VE5112 FPGA SYSTEM DESIGN LABORATORY L T P C
0 0 4 2

OBJECTIVE:

FPGAs are important platform used throughout the industry both in their own right in building complete systems. They are also used as validation/verification platforms prior to undertaking cost and time intensive design and fabrication of custom VLSI designs. Starting from high level design entry in the form VHDL/Verilog codes, the students will be carrying out complete hardware level FPGA validation of important digital algorithms.

EXPERIMENTS:

1. Design Entry Using VHDL or Verilog using HDL languages of
   i. Combinational circuits namely 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder.
   ii. Sequential circuits namely D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters.
2. Test vector generation and timing analysis of sequential and combinational logic design in (1).

3. Synthesis, P&R and post P&R simulation of the components simulated in (1) above. Critical paths to be identified. Identify and verify possible conditions under which the blocks will fail to work correctly.
4. **FPGA implementation of PCI Bus & arbiter.**
5. Interfacing with Memory modules in FPGA Boards.
6. **Realization of Discrete Fourier transform/Fast Fourier Transform algorithm in HDL and observing the spectrum in simulation.**
7. Verification of design functionality implemented in FPGA by capturing the signal in DSO.
8. Verifying design functionality using either chipscope feature (Xilinx) /the signal tap feature (Altera)/other equivalent feature . Invoke the PLL and demonstrate the use of the PLL module for clock generation in FPGAs.

TOTAL : 60 PERIODS

COURSE OUTCOMES:

At the end of the course, the student should be able to

CO1: Write HDL codes for digital circuits satisfying given specification.

CO2: Import the logic modules into FPGA Boards.

CO3: Synthesis, Place and Route the digital IPs.

CO4: Use FPGA EDA tools for design and analysis.

CU5092 REAL TIME EMBEDDED SYSTEMS LT P C
3 0 0 3

OBJECTIVES:

- To study the basic concepts of ARM processors
- To understand the computing platform and design analysis of ARM processors
- To study the concepts of Operating systems in ARM
- To study the concept of embedded networks
- To understand case studies related to embedded systems

UNIT I INTRODUCTION TO ARM PROCEESORS 9

Fundamentals of ARM, ARM Instruction set, Thumb Instruction set, ARM assembly language programming, Digital Signal Processing in ARM, Exceptions & Interrupt Handling.

UNIT II COMPUTING PLATFORM AND DESIGN ANALYSIS 9

CPU buses – Memory devices – I/O devices – Memory Protection Units – Memory Management Units – Component interfacing – Design with microprocessors – Development and Debugging – Program design – Model of programs – Assembly and Linking – Basic compilation techniques – Analysis and optimization of execution time, power, energy, program size – Program validation and testing.

UNIT III PROCESS AND OPERATING SYSTEMS 9

Multiple tasks and multi processes – Processes – Context Switching – Scheduling policies - Multiprocessor – Inter Process Communication mechanisms – Evaluating operating system performance – Power optimization strategies for processes – Firmware and Operating Systems for ARM processor.

UNIT IV HARDWARE ACCELERATES & NETWORKS 9

Accelerators – Accelerated system design – Distributed Embedded Architecture – Networks for Embedded Systems – Network based design – Internet enabled systems.

UNIT V CASE STUDY **9**

Hardware and software co-design - Data Compressor - Software Modem – Personal Digital Assistants – Set–Top–Box. – System-on-Silicon – FOSS Tools for embedded system development.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of this course, the student should be able to:

- Revise computing platform and design analysis
- Demonstrate multiple tasks and multi processes
- Discuss hardware and software co-design

REFERENCES:

1. Andrew N Sloss, Dominic Symes and Chris Wright, “ARM System Developer’s guide – Designing and Optimizing System Software”, Morgan Kaufmann publishers, 2004.
2. David E-Simon, “An Embedded Software Primer”, Pearson Education, 2007.
3. K.V.K.K.Prasad, “Embedded Real-Time Systems: Concepts, Design & Programming”, dreamtech press, 2005.
4. Tim Wilmshurst, “An Introduction to the Design of Small Scale Embedded Systems”, Pal grave Publisher, 2004.
5. Wayne Wolf, “Computers as Components - Principles of Embedded Computer System Design”, Morgan Kaufmann Publisher, 2006.

VL5291 VLSI SIGNAL PROCESSING **L T P C**
3 0 0 3

OBJECTIVES:

- To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
- To introduce efficient design of DSP architectures suitable for VLSI

UNIT I PIPELINING AND PARALLEL PROCESSING OF DIGITAL FILTERS **9**

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II ALGORITHMIC STRENGTH REDUCTION TECHNIQUE I **9**

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT III ALGORITHIMIC STRENGTH REDUCTION -II **9**

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with powerof-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES **9**

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon‟s bit-serial multipliers using Horner‟s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V NUMERICAL STRENGTH REDUCTION, WAVE AND ASYNCHRONOUS PIPELINING 9

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

TOTAL: 45 PERIODS

COURSE OUTCOME:

- Ability to modify the existing or new DSP architectures suitable for VLSI.

REFERENCES:

1. Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design and implementation ", Wiley, Interscience, 2007.
2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable Gate Arrays", Springer, 2nd Edition, 2004.

VE5201 HARDWARE SOFTWARE CO DESIGN OF EMBEDDED SYSTEM L T P C
3 0 0 3

OBJECTIVES:

- To introduce the key concepts of hardware/software communication to make trade-offs between the flexibility and the performance of a digital system.
- To learn the concept of integration of custom hardware components with software.
- Students will gain design and implementation experience with case studies.

UNIT I NATURE OF HARDWARE AND SOFTWARE 9

Hardware, Software, Definition of Hardware/Software Co-Design – Driving factors Platform design space – Application mapping – Dualism of Hardware design and software design – Concurrency and parallelism, Data flow modeling and Transformation – Data Flow Graph – Tokens, actors and queues, Firing rates, firing rules and Schedules – Synchronous data flow graph – control flow modeling – Adding time and resources – Trandformations.

UNIT II DATA FLOW IMPLEMENTATION IN SOFTWARE AND HARDWARE 9

Software Implementation of Data Flow – Converting queues and actors into software, Dynamic Scheduler – Hardware Implementation of Data Flow – single rate SDF graphs into hardware, Pipelining – Analysis of control flow and data flow – construction of control and data flow graph – Translating C into hardware – Designing data path and controller.

UNIT III DESIGN SPACE OF CUSTOM ARCHITECTURES 9

Finite state machines with datapath – FSMD design example, Limitations – Microprogrammed Architecture – Microprogrammed control, microinstruction encoding, Microprogrammed data path, microprogrammed machine – General purpose Embedded Core – RISC pipeline, Program organization – SoC interfaces for custom hardware – Design Principles in SoC Architecture

UNIT IV HARDWARE/ SOFTWARE INTERFACES 9

Principles of Hardware/software communication – synchronization schemes, communication constrained versus Computation constrained, Tight and Loose coupling - On-chip buses – Memory mapped interfaces – coprocessor interfaces – custom instruction interfaces – Coprocessor hardware interface – Data and control design, programmer's model.

UNIT V CASE STUDIES 9

Trivium Cripto coprocessor – Trivium stream cipher algorithm, Trivium for 8-bit platforms – AES coprocessor, CORDIC coprocessor – algorithm and implementation.

TOTAL:45 PERIODS

COURSE OUTCOMES:

On completion of the course, a student should be able:

- To analyze and apply design methodologies.
- To appreciate the fundamental building blocks of the using hardware and software co-design and related implementation and testing environments and techniques and their interrelationships.
- To be familiar with modern hardware/software tools for building prototypes and to be able to demonstrate practical competence in these areas

REFERENCES:

1. Ralf Niemann, “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Pub, 1998.
2. Jorgen Staunstrup, Wayne Wolf, ”Hardware/Software Co-Design: Principles and Practice”, Kluwer Academic Pub, 1997.
3. Giovanni De Micheli, Rolf Ernst Morgon, ”Reading in Hardware/Software Co-Design“ Kaufmann Publishers, 2001.
4. Patrick Schaumont, A Practical Introduction to Hardware/Software Codesign, Springer, 2nd Edition, 2010.

VL5202 LOW POWER VLSI DESIGN L T P C

3 0 0 3

OBJECTIVES:

- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent
- Power dissipation mechanism in various MOS logic style.
- Identify suitable techniques to reduce the power dissipation.
- Design memory circuits with low power dissipation.

UNIT I POWER DISSIPATION IN CMOS 9

Physics of power dissipation in CMOS FET devices – Hierarchy of limits of power – Sources of power consumption – Static Power Dissipation, Active Power Dissipation - Designing for Low Power, Circuit Techniques For Leakage Power Reduction - Basic principle of low power design.

UNIT II POWER OPTIMIZATION 9

Logic level power optimization – Circuit level low power design – Standard Adder Cells, CMOS Adders Architectures-BiCMOS adders - Low Voltage Low Power Design Techniques, Current Mode Adders -Types Of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer arithmetic techniques for low power system – low voltage low power static Random access and dynamic Random access memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.

UNIT IV POWER ESTIMATION 9

Power Estimation techniques – logic power estimation – Simulation power analysis –Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 9

Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

- The student will get to know the basics and advanced techniques in low power design which is a hot topic in today"s market where the power plays major role.
- The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.

REFERENCES:

1. AbdelatifBelaouar, Mohamed.I.Elmasry, “Low power digital VLSI design”, Kluwer, 1995.
2. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995.
3. DimitriosSoudris, C.Pignet, Costas Goutis,“Designing CMOS Circuits for Low Power”Kluwer, 2002.
4. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.
5. James B.Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, John Wiley and sons, inc. 2001.
6. J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley 1999.
7. Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2000.
8. Kiat-send Yeo, Kaushik Roy “Low-Voltage, Low-power VLSI Subsystem”, Tata McGraw-Hill, 2009.

VE5211	EMBEDDED SYSTEMS DESIGN LABORATORY	L	T	P	C
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OBJECTIVES:

- Students have knowledge about the basic functions of embedded systems.
- Students have knowledge in programming skills.

EXPERIMENTS :

ATMEGA / RASPBERRY PI Microcontroller based Experiments with MPLAB IDE from Microchip/ µVision IDE for ARM programming from Keil:

1. Interfacing basic digital input output devices.
2. Interfacing a character LCD.
3. Interfacing A/D and D/A converter.
4. Interfacing Capture/Compare/PWM module
5. Interfacing with USB/WIFI/BLE.
6. DC motor control.
7. Multiplexing seven segment LED displays.
8. Interfacing Stepper motor and temperature sensor.
9. Traffic light controller using Keil real time Kernel.
10. IoT System Design

TOTAL : 60 PERIODS

COURSE OUTCOMES:

- An ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, and sustainability.

VE5001 VLSI ARCHITECTURES FOR SYSTEM DESIGN L T P C
3 0 0 3

OBJECTIVES:

- This course will introduce the features, programming and applications of programmable logic devices.
- Provide VLSI system design experience using FSM.
- Discuss the various implementation strategies with FPGA.

UNIT I PROGRAMMABLE LOGIC 9

ROM, PLA, PAL, PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series, CPLD, Cypres FLASH 370 Device Technology, Lattice LSI's Architectures – 3000 Series – Speed Performance and in system programmability.

UNIT II FPGAS: FIELD PROGRAMMABLE GATE ARRAYS 9

Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs, Case studies – Xilinx Virtex-6, Spartan-6 FPGAs, ALTERA's FLEX 8000/10000 FPGAs, NIOS II Embedded Processor, ACTEL's IGLOO series, ProASIC3 series FPGAs.

UNIT III FINITE STATE MACHINES (FSM) 9

Top Down Design – State Transition Table, state assignments for FPGAs. Problem of initial state assignment for one hot encoding. Derivations of state machine charges. Realization of state machine charts with a PAL. Alternative realization for state machine chart using microprogramming. Linked state machines. One – Hot state machine, Petrinetes for state machines – basic concepts, properties. Extended petrinets for parallel controllers. Finite State Machine – Case Study, Meta Stability, Synchronization - Clock and reset domain crossing.

UNIT IV FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN 9

Architectures centered around non-registered PLDs. State machine design centered around shift registers. One – Hot design method. Use of ASMs in One – Hot design. K Application of One – Hot method. System level design – controller, data path and functional partition.

UNIT V IMPLEMENTING APPLICATIONS WITH FPGAS 9

Strengths and Weaknesses of FPGAs, Application and computational Characteristics and Performance - General Implementation Strategies for FPGA-based Systems - Configure-once Runtime Reconfiguration Design Flow –.Implementing Arithmetic - Fixed-point, Floating- point, Block Floating Point number Representation - CORDIC Architectures for FPGA Computing.

TOTAL:45 PERIODS

COURSE OUTCOMES:

After the completion of this course, the students are to:

- Be able to make the system level designs using FSM and analyze the performance with FPGA.

REFERENCES:

1. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall (Pte), 1994.
2. S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Publications, 1994.
3. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.
4. S.Brown, R.Francis, J.Rose, Z.Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.
5. Scott Hauck and Andre DeHon, "Reconfigurable Computing The Theory and Practice of FPGA based Computation", Morgan Kaufmann Publishers, 2008.

VE5002 PARALLEL AND RECONFIGURABLE ARCHITECTURES L T P C
3 0 0 3

OBJECTIVES:

- The student shall develop an overview and deeper insight into the research and development that is underway to meet future needs of flexible processor solution, for energy efficient reconfigurable architectures with high computing performance.

UNIT I INTRODUCTION 9

Reconfigurable Computing Systems (RCS) – Evolution of reconfigurable systems – Characteristics of RCS - Advantages and issues, Fundamental concepts & Design steps, Domain specific processors, Application specific processors, Classification of reconfigurable architecture - fine, coarse grain & hybrid architectures

UNIT II PARALLEL AND ADVANCED PROCESSORS 9

Classification of parallel computers, Multiprocessors and multicomputer, SIMD Processing Architectures, CISC & RISC Processors, VLIW Architectures

UNIT III RECONFIGURABLE ARCHITECTURES 9

FPGA Technology and Architectures – LUT devices and mapping (Look-up Table) ALU design – Placement and partitioning algorithms – Routing algorithms, Spatial Computing Architectures – Systolic Architectures and Algorithms Systolic Structures

UNIT IV RECONFIGURATION MANAGEMENT 9

Reconfiguration, Configuration Architectures, Managing the Reconfiguration Process, Reducing Configuration Transfer Time

UNIT V CASE STUDIES OF FPGA APPLICATIONS 9

Dynamic Partial Reconfigurable FIR Filter Design, Trigonometric Computing, Embedded in a Dynamically Reconfigurable CORDIC System-on-Chip, A Fast Run Time Reconfigurable Platform for Image Edge Detection, Efficient Floating-Point Implementation of High-Order (N) LMS Adaptive Filters in FPGA, Area/Performance Improvement of NoC Architectures.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon successful completion of the course, the student should be able to:

- Analyze the different architecture principles relevant in parallel and reconfigurable systems.
- Compare the tradeoffs that are necessary to meet the area, power and timing criteria of these systems.
- In depth analysis of current research projects to get broader context and assess its significance.
- Describe and relate new architectures and applications in relations to the previously existing solutions.

REFERENCES:

1. Christophe Bobda, “Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications”, Springer, 2007.
2. Scott Hauck and Andre Dehon, “Reconfigurable Computing: The Theory and Practice of FPGA based Computation”, Elseiver, 2008.
3. Niccolo Battezzatti, Luca Sterpone, Massimo Violante, “Reconfigurable Field Programmable Gate Arrays for Mission-Critical Applications”, Springer, 2011.
4. Kai Hwang, “Advanced computer architecture – Parallelism, Scalability, Programmability”; Tata McGraw Hill Publishing company Ltd., New Delhi, 1993.
5. Koen Bertels, João M.P. Cardoso, Stamatis Vassiliadis, “Reconfigurable Computing: Architectures and Applications”, Springer, 2006.
6. Kai Hwang and Zu, “Scalable Parallel Computers Architecture”, McGraw Hill Publishing Ltd., 1997.

VE5003 ADVANCED CMOS ANALOG IC DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To provide the fundamental concepts of noise in IC, OTA design, switched-capacitor circuits and data conversion circuits.

UNIT I NOISE IN INTEGRATED CIRCUITS 9

Statistical Characteristics of Noise, Sources of noise, noise models of IC components, Circuit noise calculations, equivalent input noise generators, effect of feedback on noise performance, noise in CS, CE, CG and cascode amplifiers, noise in differential pair, noise bandwidth.

UNIT II OTA DESIGN CONSIDERATION 9

Step response, Slewing, OTA variations, CMFB implementation, Input resistance, Output resistance, Output Voltage swing, CMRR, PSRR of two-stage telescopic amplifiers.

UNIT III BANDGAP REFERENCE CIRCUIT AND SWITCHED CAPACITOR CIRCUITS 9

Supply Insensitive biasing, Temperature insensitive biasing, Sampling Switches, Speed Considerations, Precision Considerations, Charge Injection Cancellation, Switched-Capacitor Amplifiers, Switched- Capacitor Integrator, Switched-Capacitor Common-Mode Feedback.

UNIT IV PERFORMANCE METERICS OF DATA CONVERTERS & NYQUIST RATE D/A CONVERTERS 9

Ideal Sampling, Reconstruction, Quantization, Static performance metrics, Dynamic performance metrics, Current Steering DACs, capacitive DACs, Binary weighted versus thermometer DACs.

UNIT V ANALOG TO DIGITAL CONVERTERS 9

Single stage amplifier as comparator, resistor-based latched comparators. offset cancellation, Flash ADC, Successive approximation ADC, Pipelined ADC, Time Interleaved ADC.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the completion of the subject, students should:

- Be able to grasp the fundamental concept of noise in IC.
- Be able to study and analyze switched-capacitor circuits and the issue of non-linearity and mismatch in the circuits.
- Be able to analyze data conversion circuits such as DAC and ADC and their design techniques.

REFERENCES:

1. Gray, Hurst, Lewis, Meyar, “Analysis and Design of Analog Integrated Circuits” 5th Edition John Wiley, 2009.
2. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw Hill, 12th Reprint, 2012.
3. Rudy Van de Plassche, “CMOS Integrated ADC and DACs”, Springer, 2nd Edition, 2007
4. Phillip E.Allen, DouglasR.Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 3rd Edition, 2011.
5. Jacob Baker “CMOS: Circuit Design, Layout, and Simulation”, Wiley IEEE Press, 3rd Edition, 2010.

VE5004 DISTRIBUTED EMBEDDED COMPUTING L T P C
3 0 0 3

OBJECTIVES:

- To expose the students to the fundamentals of Network communication technologies.
- To teach the fundamentals of Internet
- To study on Java based Networking
- To introduce network routing Agents
- To study the basis for network on-chip technologies

UNIT I THE HARDWARE INFRASTRUCTURE 9

Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – Wide Area Networks – Network management – Network Security – Cluster computers.

UNIT II INTERNET CONCEPTS 9

Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

UNIT III DISTRIBUTED COMPUTING USING JAVA 9

IO streaming – Object serialization – Networking – Threading – RMI – multicasting – distributed databases – embedded java concepts – case studies.

UNIT IV EMBEDDED AGENT 9

Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks embedded-agent. Case study: Mobile robots.

UNIT V EMBEDDED COMPUTING ARCHITECTURE 9

Synthesis of the information technologies of distributed embedded systems – analog/digital co-design – optimizing functional distribution in complex system design – validation and fast prototyping of multiprocessor system-on-chip – a new dynamic scheduling algorithm for real-time multiprocessor systems.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

At the completion of the course, students will be able to:

- Explain the fundamentals of Network communication technologies, internet, and Java based networking.
- Analyze the analog/digital co-design of distributed embedded computing architecture.

REFERENCES:

1. Dietel & Dietel, “JAVA how to program”, Prentice Hall, 1999.
2. Sape Mullender, “Distributed Systems”, Addison-Wesley, 1993.
3. George Coulouris and Jean Dollimore, “Distributed Systems – concepts and design”,Addison –Wesley, 1988.
4. “Architecture and Design of Distributed Embedded Systems”,Bernd Kleinjohann C-lab, Universitat Paderborn, Germany, Kluwer Academic Publishers, Boston, 2001.

VE5005 COMPUTER AIDED DESIGN FOR VLSI CIRCUITS L T P C
3 0 0 3

OBJECTIVES:

- To discuss the Algorithmic Graph Theory and computational complexity optimization.
- To discuss the concepts of layout design rules and floor planning.
- To simulate and synthesis different hardware models.

UNIT I VLSI DESIGN METHODOLOGIES 9

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II DESIGN RULES 9

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms – partitioning.

UNIT III FLOOR PLANNING 9

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV SIMULATION 9

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis - Circuit and AMS Co-Simulation techniques.

UNIT V MODELLING AND SYNTHESIS 9

High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations, Analog Behavioural Modelling for Simulation, Low Power Simulation .

TOTAL : 45 PERIODS

COURSE OUTCOMES:

At the completion of this subject,

- Students will be able to implement, simulate and synthesis the computer aided design of VLSI systems.

REFERENCES:

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons,2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

VE5006 DIGITAL IMAGE AND VIDEO PROCESSING L T P C
3 0 0 3

OBJECTIVES:

- To provide the basic concepts of image & pattern recognition.
- To give an exposure to basic image processing and modeling techniques.
- To provide an understanding of various concepts related to video object extraction.
- To prepare students for development and implementation of algorithms

UNIT I IMAGE FUNDAMENTALS AND TRANSFORMS 9

Image Representation- Sampling and Quantization - Two dimensional DFT- Discrete cosine Transform - Walsh - Hadamard transform - Wavelet transform - Construction of Wavelets-Types of wavelets - principal component analysis.

UNIT II PROCESSING AND MODELING OF IMAGES 9

Pre-processing -Point operations – contrast stretching – Histogram - Histogram equalization - Image segmentation- pixel based, edge based, region based segmentation - Morphological image processing - Edge and texture models - Image registration - Colour Image Processing -

UNIT III SPATIAL FEATURE EXTRACTION 9

Feature selection - Localized feature extraction- Boundary Descriptors - Moments - Texture Descriptors - Co-occurrence features

UNIT IV CLASSIFIERS 9

Kernel based approaches - clustering methods - Maximum Likelihood Estimation- Bayesian approach- Pattern Classification

UNIT V VIDEO OBJECT EXTRACTION 9

Back ground subtraction – Frame difference - Static and dynamic background modeling - optical flow techniques-Handling occlusion- scale and appearance changes - Shadow removal.

TOTAL :45 PERIODS

COURSE OUTCOMES:

- To be able to design pattern recognition systems.
- To design and implement feature extraction techniques for a given application.
- To design a suitable classifier for a given application.

REFERENCES:

1. A.K.Jain, “Fundamentals of Digital Image Processing”, Prentice-Hall, 2002.
2. R.C.Gonzalez and R.E.Woods, “Digital Image Processing”, Pearson Education, 2nd Edition, 2002.
3. A.Bovik, “Handbook of Image and Video Processing”, Academic Press, 2nd Edition, 2005.
4. Mark Nixon and Alberto Aguado, “Feature Extraction and Image Processing”, Academic Press, 2008.
5. John C.Russ, “The Image Processing Handbook”, CRC Press, 2007.
6. Richard O. Duda, Peter E. Hart and David G. Stork., “Pattern classification”, Wiley, 2001.

VE5007 ALGORITHMS FOR VLSI DESIGN AUTOMATION L T P C
3 0 0 3

OBJECTIVES:

- To discuss the algorithms for logic synthesis, verification.
- To discuss about the design tradeoff in various partitioning algorithms, placement, floor planning and pin assignment of VLSI design automation.
- To analyze the different global routing algorithms and compaction in design automation.

UNIT I LOGIC SYNTHESIS & VERIFICATION: 6

Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis, Introduction to Circuit Simulation - Co - Simulation.

UNIT II PARTITIONING: 9

Problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

UNIT III PLACEMENT, FLOOR PLANNING & PIN ASSIGNMENT: 9

Problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

UNIT IV GLOBAL ROUTING: 12

Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches Detailed Routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms Over The Cell Routing & Via Minimization: two layers over the cell routers, constrained & unconstrained via minimization.

UNIT V COMPACTION: 9

Problem formulation, one-dimensional compaction, two dimensions based compaction, hierarchical compaction.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Ability to analyze the algorithms needed for synthesis, partitioning, placement, floor planning, routing in VLSI design automation

REFERENCES:

1. Naveed Shervani, “Algorithms for VLSI physical design Automation”, Kluwer Academic Publisher, Second edition.
2. Christophn Meinel & Thorsten Theobold, “Algorithm and Data Structures for VLSI Design”, KAP, 2002.
3. Rolf Drechsheler : “Evolutionary Algorithm for VLSI CAD”, Kluwer Academic publisher, 2nd Edition, 1998.
4. Trimburger, “Introduction to CAD for VLSI”, Kluwer Academic publisher, 2002
5. Sabih H.Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2007

VE5008 ADVANCED EMBEDDED SYSTEM DESIGN L T P C
3 0 0 3

OBJECTIVES

- To teach the fundamentals on design attributes of functional units of embedded systems.
- To discuss about Hardware, software partitioning in system design
- To introduce architectural features of 32 bit ARM microcontroller.
- To discuss strategies for embedded firmware design and development.
- To develop an integrated development environment in embedded system

UNIT I TYPICAL EMBEDDED SYSTEM 9

Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Characteristics and Quality Attributes of Embedded Systems: Hardware, Software Co-Design and Program Modeling, RISC V, Computational Models in Embedded Design, Introduction to Unified Modeling Language, Hardware Software -

UNIT II EMBEDDED HARDWARE DESIGN AND DEVELOPMENT 9

EDA Tools, How to Use EDA Tool, Schematic Design – Place wire, Bus , port, junction, creating part numbers, Design Rules check, Bill of materials, Netlist creation , PCB Layout Design – Building blocks, Component placement.

UNIT III ARM -32 BIT MICROCONTROLLER FAMILY 9

Architecture of ARM Cortex M3 –General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Register,. Nested Vector Interrupt Controller. Interrupt behavior of ARM Cortex M3. Exceptions Programming. Advanced Programming Features. Memory Protection. Debug Architecture.

UNIT IV EMBEDDED FIRMWARE DESIGN AND DEVELOPMENT 9

Embedded Firmware Design Approaches, Embedded Firmware Development Languages, Real-Time Operating System (RTOS) based Embedded System Design: Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS

UNIT V EMBEDDED SYSTEM DEVELOPMENT ENVIRONMENT 9

The Integrated Development Environment (IDE), Types of Files Generated on Cross compilation, Disassembler/ELDompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan - Hardware Security, Software Security.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

- Ability to discuss the concepts of typical embedded systems.
- Ability to develop an integrated development environment of hardware/software codesign of embedded system.

REFERENCES:

1. Shibu K V, “Introduction to Embedded Systems”, Tata McGraw Hill Education Private Limited, 2009
2. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, Newnes, (Elsevier), 2008.
3. James K Peckol, “Embedded Systems – A contemporary Design Tool”, John Weily, 2008.
4. David. A.Patterson & John L. Hennessy, "Computer Organisation and Design : the Hardware and Software Interface:RISC - V, Morgan Kaufmann, 1st Edition, 2017.

VE5009 POWER MANAGEMENT AND CLOCK DISTRIBUTION CIRCUITS L T P C
3 0 0 3

OBJECTIVES:

- To teach the design of reference circuits and low drop out regulators for desired specifications
- To teach oscillator choice and requirements for clock generation circuits
- To teach the design of clock generation and recovery in the context of high speed systems

UNIT I VOLTAGE AND CURRENT REFERENCES 9

Current Mirrors, Self Biased Current Reference, startup circuits, VBE based Current Reference, VT Based Current Reference, Band Gap Reference , Supply Independent Biasing, Temperature Independent Biasing, PTAT Current Generation, Constant Gm Biasing

UNIT II LOW DROP OUT REGULATORS 9

Analog Building Blocks, Negative Feedback, Performance Metrics, AC Design, Stability, Internal and External Compensation, PSRR – Internal and External compensation circuits.

UNIT III OSCILLATOR FUNDAMENTALS 9

General considerations, Ring oscillators, LC oscillators, Colpitts Oscillator, Jitter and Phase noise in Ring Oscillators, Impulse Sensitivity Function for LC & Ring Oscillators, Phase Noise in Differential LC Oscillators.

UNIT IV CLOCK DISTRIBUTION CIRCUITS 9

PLL Fundamental, PLL stability, Noise Performance, Charge-Pump PLL Topology, CPPLL Building blocks, Jitter and Phase Noise performance, DLL fundamentals.

UNIT V CLOCK AND DATA RECOVERY CIRCUITS 9

CDR Architectures, Trans Impedance Amplifiers and Limiters, CMOS Interface, Linear Half Rate CMOS CDR Circuits, Wide capture Range CDR Circuits.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Design Band gap reference circuits and Low Drop Out regulator for a given specification.
CO2: Understand specification related to Supply and Clock generation circuits of ICs
CO3: Choose oscillator topology and design meeting the requirement of clock generation circuits.
CO4: Design clock generation circuits in the context of high speed I/Os, High speed Broad Band Communication circuits and Data Conversion Circuits.

REFERENCES:

1. Gabriel.A. Rincon-Mora, "Voltage references from diode to precision higher order bandgapcircuits", Johnwiley& Sons, Inc 2002.
2. Gabriel.A. Rincon-Mora, "Analog IC Design With Low-Dropout Regulators", McGraw-Hill Professional Pub, 2009.
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001
4. Floyd M. Gardner ,"Phase LocK Techniques" John wiley& Sons, Inc 2005.
5. Michiel Steyaert, Arthur H.M. van Roermund, Herman Casier, "Analog Circuit Design: High Speed Clock and Data Recovery, High-performance Amplifiers Power Management" springer, 2008.
6. BehzadRazavi, " Design of Integrated circuits for Optical Communications", McGraw Hill, 2003.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	1	2	2
CO2	3		3	1	2	2
CO3	3		3	1	2	2
CO4	3		3	1	2	2

VE5010 ADAPTIVE SIGNAL PROCESSING L T P C
3 0 0 3

OBJECTIVES:

- To provide an in-depth coverage of the adaptive filter theory.
- To provide the mathematical framework for the understanding of adaptive statistical signal processing.
- To know the basic tools of vector spaces and discrete-time stochastic process.
- To understand the various issues involved in adaptive filtering.
- Various types of adaptive filters will be introduced and their properties will be studied, specifically convergence, tracking, robustness and computational complexity.
- Learn to apply adaptive filter theory using prescribed case studies.

UNIT I STOCHASTIC PROCESSES AND SPECTRUM ESTIMATION 9

Statistical characteristics of a stochastic process-Non-Parametric methods - Correlation method - Covariance estimator - Performance analysis of estimators – Unbiased consistent estimators -Periodogram estimator - Barlett spectrum estimation - Welch estimation - Model based approach -AR, MA, ARMA Signal modeling - Parameter estimation using Yule-Walker method.

UNIT II WIENER FILTERS 9

Optimum Filtering-The normal equations and the Wiener filter-Minimum mean square error estimation and the orthogonality principle- Wiener-Hopf equations- Linear prediction-forward Linear PredictionBackward linear prediction-Levinson-Durbin algorithm.

UNIT III GRADIENT-BASED ADAPTIVE FILTERS 9

The basic idea of the steepest descent algorithm- The steepest descent algorithm applied to wiener filter – Stability of the steepest descent algorithm- The LMS algorithm-LMS adaptive algorithm-Method of Least Squares-Data windowing-Properties of LS Estimates-MVDR spectrum estimation. Recursive Least Squares (RLS)-Exponentially weighted RLS-Convergence analysis-Sliding window RLS.

UNIT IV KALMAN FILTERS & TRACKING 9

Statement of the Kalman filtering problem-The innovation process- Estimation– Filtering - Initial conditions. Variants of the Kalman filter-The Extended Kalman filter-Criteria for tracking assessment, Tracking performance of the LMS and RLS algorithms- Comparison.

UNIT V APPLICATIONS 9

Channel equalization-Echo cancellation- Deconvolution- Adaptive noise cancellation-Adaptive interference cancellation. Case study.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

- To be able to solve the problems related to optimal design, convergence, and recursiveness.
- To carry out time/frequency domain implementations of adaptive filters.
- To be able to apply the concepts of stochastic processes to adaptive filters.
- To be able to design adaptive filter algorithms.
- To be able to apply adaptive filter theory to applications such as echo cancelation, noise cancellation and channel equalization.

REFERENCES:

1. Simon Haykin, “Adaptive Filter Theory”, Pearson Education, 4th Edition, 2003.
2. Monson H. Hayes, “Statistical Digital Signal Processing and Modeling”, Wiley, 2008.
3. Ali.H.Sayed, “Fundamentals of Adaptive Filtering”, John Wiley & Sons, 2003.
4. Paulo S. R. Diniz, “Adaptive Filtering Algorithms and Practical Implementation”, Springer, 2011.
5. Lino Garcia, “Adaptive Filtering Applications”, InTech, Published, 2011.
6. Kong-Aik Lee, Woon-Seng Gan, Sen M. Kuo, “Subband Adaptive Filtering: Theory and Implementation”, Wiley, 2009.

VE5011 DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES L T P C
3 0 0 3

OBJECTIVES:

- To understand the architecture and programming of fixed and floating point DSP processors.
- To understand the techniques involved in real time DSP system design and to design and implement a variety of DSP algorithms for real world applications.
- To gain the practical knowledge of real time implementation issues.
- Learn the basic forms of FIR and IIR filters, and design filters with desired frequency responses.
- Understand the fast implementation schemes of DFT.
- Learn to apply adaptive filter theory and implement it in DSP Processor.

UNIT I INTRODUCTION TO DIGITAL SIGNAL PROCESSING SYSTEMS 9

Fundamentals of DSP - Digital signal processor architectures – Software developments – Hardware issues – System considerations – Implementation considerations, Data representations, Finite word length effects, Programming issues, Real time implementation considerations.

UNIT II FIXED AND FLOATING POINT DIGITAL SIGNAL PROCESSORS 9

TMS320C55x – Architecture overview, Addressing modes, Instruction set, Programming considerations, system issues. TMS320C62x AND TMS320C64x - Architecture overview, Memory systems, External memory addressing, Instruction set, Programming considerations, system issues. TMS320C67X – Architecture overview, Instruction set, Pipeline Architecture, Programming considerations, Realtime implementations.

UNIT III FAST FOURIER TRANSFORMS 9

Introduction to DFT – FFT algorithms – Decimation-in-time, Decimation-in-frequency - Fixed point implementation using TMS320C64x, Floating point implementation using TMS320C67x.

UNIT IV FIR AND IIR FILTER IMPLEMENTATIONS 9

FIR and IIR filters – Characteristics, Structures, FIR Filter design using Windowing and frequency sampling method, IIR Filter-Butterworth and Chebyshev Filter Design-, Fixed point implementation using TMS320C64x, Floating point implementation using TMS320C67x.

UNIT V ADAPTIVE FILTER STRUCTURES AND ALGORITHMS 9

Wiener filter, LS filter , Filter structures, Adaptive algorithms, Properties and Applications – Fixed and floating point implementation using TMS320C64x and TMS320C67x.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

- To be able to develop the program for fixed and floating point DSP processors based on the design issues.
- To be able to design and develop real time implementations on DSP algorithms.
- Ability to design IIR and FIR filters.
- To apply the fast transforms for the analysis of DSP systems.
- To be able to realize and implement a suitable structure for FIR and IIR Filters.
- To be able to design adaptive filter algorithms.

REFERENCES:

1. Sen M.Kuo, Woon-Seng S.Gan, “Digital Signal Processors – Architectures, Implementations and Applications”, Pearson Education, 2005, Second Impression, 2009.
2. Lapsley et al “DSP Processor Fundamentals, Architectures & Features”, S.Chand & Co, Reprint, 2000.
3. Monson H. Hayes, “Statistical Digital Signal Processing and Modeling”, Wiley, 2008.
4. John G Proakis and Manolakis, “Digital Signal Processing Principles, Algorithms and Applications”, Pearson, 4th Edition, 2007.
5. TMS Manual on TMS320C64XX and TMS320C67XX.

6. A.V. Oppenheim, R.W.Schafer and J.R.Buck, "Discrete Time Signal Processing", Pearson, 2004.
7. S.K. Mitra, “Digital Signal Processing, A Computer Based approach", Tata McGraw-Hill, 1998.
8. P.P. Vaidyanathan, “Multirate Systems & Filter Banks", Prentice Hall, 1993.
9. I.C.Ifeachor and B.W. Jervis, “Digital Signal Processing-A Practical Approach”, Pearson, 2002.

CU5073 VLSI FOR WIRELESS COMMUNICATION L T P C

3 0 0 3

OBJECTIVES:

- To understand the concepts of basic wireless communication concepts.
- To study the parameters in receiver and low noise amplifier design.
- To study the various types of mixers designed for wireless communication.
- To study and design PLL and VCO.
- To understand the concepts of transmitters and power amplifiers in wireless communication.

UNIT I COMMUNICATION CONCEPTS 9

Introduction – Overview of Wireless systems – Standards – Access Methods – Modulation schemes – Classical channel – Wireless channel description – Path loss – Multipath fading – Standard Translation.

UNIT II RECEIVER ARCHITECTURE & LOW NOISE AMPLIFIERS 9

Receiver front end – Filter design – Non-idealities – Design parameters – Noise figure & Input intercept point. LNA Introduction – Wideband LNA design – Narrow band LNA design: Impedance matching & Core amplifier.

UNIT III MIXERS 9

Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion – Noise - A Complete Active Mixer. Switching Mixer – Distortion, Conversion Gain & Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain, Distortion, Intrinsic & Extrinsic Noise in Single Ended Sampling Mixer.

UNIT IV FREQUENCY SYNTHESIZERS 9

PLL – Phase detector – Dividers – Voltage Controlled Oscillators – LC oscillators – Ring Oscillators – Phase noise – Loop filters & design approaches – A complete synthesizer design example (DECT) – Frequency synthesizer with fractional divider.

UNIT V TRANSMITTER ARCHITECTURES & POWER AMPLIFIERS 9

Transmitter back end design – Quadrature LO generator – Power amplifier design.

TOTAL : 45 PERIODS

OUTCOMES:

At the end of this course, the student should be able to

- Design LNA and Mixers
- Evaluate frequency synthesizers
- Design and analyze power amplifiers

REFERENCES:

1. Bosco H Leung “VLSI for Wireless Communication”, Pearson Education, 2002.
2. B.Razavi ,”RF Microelectronics” , Prentice-Hall ,1998.
3. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw-Hill, 1999.
4. Emad N Farag and Mohamed I Elmasry, “Mixed Signal VLSI wireless design – Circuits & Systems”, Kluwer Academic Publishers, 2000.
5. J. Crols and M. Steyaert, “CMOS Wireless Transceiver Design,” Boston, Kluwer Academic Pub., 1997.
6. Thomas H.Lee, “The Design of CMOS Radio – Frequency Integrated Circuits”, Cambridge University Press , 2003.

VE5012	COMPUTATIONAL INTELLIGENCE	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand the fundamentals of computational intelligence
- To know about the various knowledge representation methods
- To understand the features of neural network and its implementation
- To study about various data clustering methods
- To gain knowledge in evolutionary computation and neuro – fuzzy systems

UNIT I INTRODUCTION TO COMPUTATIONAL INTELLIGENCE 9

Evolution of Computing – Introduction to Artificial Intelligence –– Turing test - Prepositional and Predicate Calculus - Expert system – Introduction – MYCIN – PROSPECTOR – Robotics – From Conventional AI to Computational Intelligence – Issues in Artificial Intelligence - Machine Learning Basics – Intelligence of ants - Artificial Life – BOTS – Comparison of various expert systems

UNIT II KNOWLEDGE REPRESENTATION METHODS 9

Introduction – rough sets – set approximation – analysis of decision tables – Application of LERS software – Type – 1 fuzzy sets – definition – basic operations on fuzzy sets – The extension principle – Triangular norms and negations – Fuzzy Relations – Approximate reasoning – fuzzy Inference systems – Application of fuzzy sets – Type – 2 fuzzy sets – Footprint of uncertainty – basic operations on fuzzy sets – Type – 2 fuzzy relations – Type reduction – type 2 fuzzy Inference systems – Comparison of Fuzzy Inference systems.

UNIT III NEURAL NETWORKS AND LEARNING ALGORITHMS 9

Machine learning using Neural Network, Adaptive Networks – Feed Forward Networks Defuzzification – Supervised Learning Neural Networks – backpropagation Algorithm – Levenberg-Marquardt algorithm – Recurrent neural networks – BAM networks - Radial Basis Function Networks - Reinforcement Learning – Unsupervised Learning Neural Networks – Adaptive Resonance Architectures – Case Study : Neural Network explanation facility.

UNIT IV DATA CLUSTERING METHODS AND ALGORITHMS 9

Introduction – Hard and fuzzy partitions – Distance Measures – Hard C- Means algorithm – Fuzzy C- Means algorithm – Possibilistic C- Means algorithm - Fuzzy Maximum Likelihood Estimates (FMLE) algorithm – Neuro Fuzzy systems - Mamdani Fuzzy Model – modelling problems - - Logical type - Takagi – Sugeno- Kang Fuzzy Model – comparison of neuro – fuzzy systems – Model evaluation criteria, complexity. Fuzzy Expert Systems – Fuzzy Decision Making – Case study: EEG spike detection.

UNIT V EVOLUTIONARY COMPUTATION AND NEURO-FUZZY SYSTEMS 9

Evolutionary computation – GA – Particle Swarm Optimization – Ant colony Optimization – Artificial Immune Systems – Honey- Bee Optimization – Memetic Algorithms - Optimization problems – TSP, JSSP - evolutionary algorithms – Flexible neuro – fuzzy systems – Introduction – soft triangular norms – Parameterized triangular norms – Adjustable triangular norms – Flexible systems – Learning algorithms – Simulation examples –Hybrid Techniques - Neuro-Fuzzy Control – Case study : Evolutionary medical diagnosis

A simple project using any one of the above domains with tools like MATLAB, Python 2 and Weka tool 3.7 .

TOTAL :45 PERIODS

COURSE OUTCOMES:

- Implement computational intelligence through applications
- Understand knowledge representation methods and apply approximate reasoning
- Apply evolutionary algorithm to solve the optimization problem
- Gain research Knowledge to develop applications using hybrid systems
- Able to Model Flexible Fuzzy Inference systems for dynamic nonlinear data sets

REFERENCES:

1. A.E. Eiben and J.E. Smith “Introduction to Evolutionary Computing” Springer, 2003
2. Andries Engelbrecht, Computational Intelligence: An Introduction, 2007
3. Amos Gilat, “ MATLAB : “An introduction with applications”, John Wiley & Sons Inc, 2011.
4. David E. Goldberg, “Genetic Algorithms in Search, Optimization and Machine Learning”, Addison Wesley, 2007
5. Elaine Rich, Kevin Knight, Shiva Shankar B. Nair, “Artificial Intelligence”, Tata McGraw hill Ltd, 2008.
6. E. Sanchez, T. Shibata, and L. A. Zadeh, Eds., "Genetic Algorithms and Fuzzy Logic Systems: Soft Computing Perspectives, Advances in Fuzzy Systems - Applications and Theory", Vol. 7, River Edge, World Scientific, 1997.
7. George J. Klir and Bo Yuan, “Fuzzy Sets and Fuzzy Logic-Theory and Applications”, Prentice Hall, 1995
8. Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, “Neuro-Fuzzy and Soft Computing”, Prentice-Hall of India, 2003
9. Kwang H.Lee, “First course on Fuzzy Theory and Applications”, Springer–Verlag Berlin Heidelberg, 2005
10. Kaluza, B. INSTANT Weka How-to, Packt Publishing, 2013.
11. Leszek Rutkowski, “ Computational Intelligence – Methods and Techniques”, Springer, 2008.
12. Mitsuo Gen and Runwei Cheng,”Genetic Algorithms and Engineering Optimization”, Wiley, Publishers 2000.
13. Mitchell Melanie, “An Introduction to Genetic Algorithm”, Prentice Hall, 1998
14. Ross Timothy J, “Fuzzy Logic with Engineering Applications”, Wiley India Pvt Ltd, New Delhi, 2010.
15. S.N.Sivanandam, S.N.Deepa, “Introduction to Genetic Algorithms”, Springer, 2007.

VE5013 **EMBEDDED C** **L T P C**
3 0 0 3

OBJECTIVES:

- To understand the basics of embedded C programming and its compilers and simulators.
- Apply to C programming in embedded systems.

UNIT I BASICS OF EMBEDDED C **9**

System programmimg Vs Application Programming-General rules in C, Comments, White Spaces, Modules, Data type, Procedures, Variables, Expression and Statements, Structures and Union, Data structures, Program Description Language.

UNIT II PROGRAMMING **9**

Adding Structure to the Code Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Examples.

UNIT III COMPLIERS AND SIMULATORS **9**

Introduction to MikroC compiler and debugger, Functions and Inbuilt libraries in MikroC, Creating new libraries, Development Tools, Introduction to simulators such as Proteus and Real PIC.

UNIT IV EMBEDDED MEMORY **9**

Mixing Assembly and C, Memory Alignment with Structures, Memory management in C, Memory-map of Applications.

UNIT V CASE STUDIES **9**

Chasing LEDs, LED Dice, Seven Segment LED Counter, Two-Digit Muliplexed Seven Segment LED Counter with Timer Interrupt, Real Time Clock, Digital Voltmeter with LCD, Calculator with Keypad and LCD, Serial Communication Based Calculator, Multitasking and Real-Time Operating Systems.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

- This subject enables our students to create, develop, apply, and disseminate the programming knowledge within the embedded systems development environment.

REFERENCES:

1. Micheal Barr, "Embedded C Coding Standard", Barr Group Publishing, 2013.
2. Milan Verle, "PIC Microcontrollers with Examples in Assembly Language", mikroElektronika Publications, 2008.
3. Milan Verle, "PIC Microcontrollers- Programming in C", mikroElektronika Publications, 2009.
4. Dogan Ibrahim, " Advanced PIC Microcontoller Projects in C- From USB to RTOS with the PIC 18F Series", Newnes Publications, 2008.
5. Mohammad Ali Mazidi, Rolin D. Mckinlay and Danny Causey, "PIC Microcontroller and Embedded Systems using Assembly and C for PIC 18", Pearson India, 2008.

VE5014 **DESIGN OF EMBEDDED CONTROL SYSTEM** **L T P C**
3 0 0 3

OBJECTIVES:

- To expose the students to the fundamentals of Embedded System Blocks
- To teach the fundamental RTOS.
- To study on interfacing for processor communication
- To compare types and Functionalities in commercial software tools
- To discuss the Applications development using interfacing

UNIT I EMBEDDED SYSTEM ORGANIZATION 9

Embedded computing, Characteristics of embedded computing applications, Embedded system design challenges, Build process of Realtime Embedded system, Selection of processor, Memory, I/O devices, Rs-485, MODEM, Bus Communication system using I2C, CAN, USB buses, 8 bit – ISA, EISA bus.

UNIT II REAL-TIME OPERATING SYSTEM 9

Introduction to RTOS, RTOS- Inter Process communication, Interrupt driven Input and Output, Nonmaskable interrupt, Software interrupt, Thread – Single, Multithread concept, Multitasking Semaphores.

UNIT III INTERFACE WITH COMMUNICATION PROTOCOL 9

Design methodologies and tools – Design flows – Designing hardware and software Interface, System Integration; SPI, High speed data acquisition and interface, SPI read/write protocol, RTC interfacing and programming.

UNIT IV DESIGN OF SOFTWARE FOR EMBEDDED CONTROL 9

Software abstraction using Mealy-Moore FSM controller, Layered software development, Basic concepts of developing device driver, SCI, Software, Interfacing & porting using standard C & C++, Functional and performance Debugging with benchmarking Real-time system software, Survey on basics of contemporary RTOS- VXWorks, UC/OS-II.

UNIT V CASE STUDIES WITH EMBEDDED CONTROLLER 9

Programmable interface with A/D & D/A interface, Digital voltmeter, Control- Robot system, PWM motor speed controller, Serial communication interface.

TOTAL : 45 PERIODS

COURSE OUTCOME:

- Students will be able to realize a real time embedded system.

REFERENCES:

1. Steven F. Barrett, Daniel J. Pack, “Embedded Systems – Design and Applications with the 68HC 12 and HCS12”, Pearson Education, 2008.
2. Raj Kamal, “Embedded Systems- Architecture, Programming and Design” Tata McGraw Hill, 2006.
3. Chattopadhyay, “Embedded System Design”,PHI Learning, 2011.
4. Steven F.Barrett,Daniel J.Pack,”Embedded Systems-Design & Application with the 68HC12 & HCS12”, Pearson Education,2008.
5. Daniel W. Lewis, “Fundamentals of Embedded Software”, Prentice Hall India, 2004.
6. Marian Andrzej Adamski, Andrei Karatkevich and Marek Wegrzyn, “ Design of Embedded control systems” Springer Science + Busciness Media, 2005.

VL5002 RF IC DESIGN L T P C

3 0 0 3

OBJECTIVES:

- To study the various impedance matching techniques used in RF circuit design.
- To understand the functional design aspects of LNAs, Mixers, PLLs and VCO.
- To understand frequency synthesis.
-

UNIT I IMPEDANCE MATCHING IN AMPLIFIERS 9

Definition of ‘Q’, series parallel transformations of lossy circuits, impedance matching using ‘L’, ‘PI’ and T networks, Integrated inductors, resistors, Capacitors, tunable inductors, transformers

UNIT II AMPLIFIER DESIGN 9

Noise characteristics of MOS devices, Design of CG LNA and inductor degenerated LNAs. Principles of RF Power Amplifiers design,

UNIT III ACTIVE AND PASSIVE MIXERS 9

Qualitative Description of the Gilbert Mixer - Conversion Gain, and distortion and noise , analysis of Gilbert Mixer – Switching Mixer - Distortion in Unbalanced Switching Mixer -Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

UNIT IV OSCILLATORS 9

LC Oscillators, Voltage Controlled Oscillators, Ring oscillators, Delay Cells, tuning range in ring oscillators, Tuning in LC oscillators, Tuning sensitivity, Phase Noise in oscillators, sources of phase noise

UNIT V PLL AND FREQUENCY SYNTHESIZERS 9

Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency Dividers, Loop Filter Design, Phase Locked Loops, Phase noise in PLL, Loop Bandwidth, Basic Integer-N frequency synthesizer, Basic Fractional-N frequency synthesizer

TOTAL: 45 PERIODS

COURSE OUTCOMES:

To understand the principles of operation of an RF receiver front end and be able to design and apply constraints for LNAs, Mixers and Frequency synthesizers.

REFERENCES:

1. B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998.
2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002.
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 1999.
4. Jia-sheng Hong, "Microstrip filters for RF/Microwave applications", Wiley, 2001.
5. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits", Cambridge University Press ,2003.

VE5015 MEMS AND MICROSYSTEMS L T P C
3 0 0 3

OBJECTIVES:

- To understand the fundamentals of MEMS and Microsystems.
- To learn MEMS accelerometers and actuators design techniques, including interfacing and packaging techniques.

UNIT I INTRODUCTION TO MEMS 9

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro accelerometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT II MICROMECHANICS 9

Elasticity, Stress, strain and material properties, Bending of thin films, Spring configurations, torsion deflection, Mechanical vibration, Resonance, Thermomechanics - actuators, force and response time, Fracture and thin film mechanics.

UNIT III MICROACTUATORS 9

Electrostatics: basic theory, electrostatic instability. Surface tension, Gap and finger pull up, Electrostatic actuators, comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators, bistable actuators.

UNIT IV INTERFACING AND PACKAGING 9

Electronic Interfaces, Feedback systems, Noise, Packaging: Dicing-Wafer level Packaging-Wafer bonding-Connections between layers-self assembly-higher level of packaging.

UNIT V CASE STUDIES 9

Optical MEMS, RF MEMS- System design basics, Case studies: Capacitive accelerometer, Peizo electric pressure sensor, MEMS scanners, Capacitive RF MEMS switch, performance issues.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of the course, students will have:

- An ability to analyze the working of MEMS and Microsystems components.
- An ability to design the MEMS accelerometer and to design Electrostatic actuators.
- An ability to analyze the working of RF and Optical MEMS.

REFERENCES:

1. Stephen D Senturia, “Microsystems Design”, Springer Publishers, 2nd Edition, 2005.
2. Nadim Maluf and Kirt Williams, “Introduction to Microelectromechanical Systems Engineering”, Artech House, 2004.
3. Mohamed Gad-el-Hak, Editor, “The MEMS Handbook”, CRC press, 2nd Edition, 2005.
4. Tai - Ran Hsu, “MEMS and Micro Systems: Design, Manufacture and Nanoscale Engineering”, Tata McGraw Hill, New Delhi, 2nd Edition, 2008.

VE5016 MULTICORE ARCHITECTURES AND PROGRAMMING L T P C
3 0 0 3

OBJECTIVES:

- To discuss the principles of different multiprocessors with their performance issues.
- To discuss the fundamentals of various programming concepts used in multicore architectures.

UNIT I INTRODUCTION TO MULTIPROCESSORS AND SCALABILITY ISSUES 9

Scalable design principles – Principles of processor design – Instruction Level Parallelism, Thread level parallelism. Parallel computer models –- Symmetric and distributed shared memory architectures – Performance Issues – Multi-core Architectures - Software and hardware multithreading – SMT and CMP architectures – Design issues – Case studies – Intel Multi-core architecture – SUN CMP architecture.

UNIT II PARALLEL PROGRAMMING 9

Fundamental concepts – Designing for threads – scheduling - Threading and parallel programming constructs – Synchronization – Critical sections – Deadlock. Threading APIs.

UNIT III OPENMP PROGRAMMING 9

OpenMP – Threading a loop – Thread overheads – Performance issues – Library functions. Solutions to parallel programming problems – Data races, deadlocks and livelocks – Non-blocking algorithms – Memory and cache related issues.

UNIT IV MPI PROGRAMMING 9

MPI Model – collective communication – data decomposition – communicators and topologies – point-to-point communication – MPI Library.

UNIT V MULTICORE ARCHITECTURES FOR EMBEDDED SYSYETMS 9

Architectural Considerations, Interconnection Networks, Software Optimizations.
Case Studies: HiBRID SoC for Multimedia Signal Processing, VIPER Multiprocesssor SoC, General Purpose Multiprocessor DSP, Multicore DSP Platforms.

TOTAL : 45 PERIODS

OUTCOMES:

- Students will be able to explain the principle and operation of multicore architectures and their programming.
- Students will be able to design a multicore architecture for an embedded system.

REFERENCES:

1. Shameem Akhter and Jason Roberts, “Multi-core Programming”, Intel Press, 2006.
2. Michael J Quinn, Parallel programming in C with MPI and OpenMP, Tata Mcgraw Hill, 2003.
3. Georgios Kornaros, “Multicore Embedded systems”, CRC Press, Taylor & Francis Group, 2010.
4. John L. Hennessey and David A. Patterson, “ Computer architecture – A quantitative approach”, Morgan Kaufmann/Elsevier Publishers, 4th Edition, 2007.
5. David E. Culler, Jaswinder Pal Singh, “Parallel computing architecture : A hardware/ software approach” , Morgan Kaufmann/Elsevier Publishers, 1999.
6. Bryon Moyer, “Real world Multicore Embedded systems”, Elsevier, 2013.
7. Gerassimos Barlas, “Multicore and GPU Programming: An Integrated Approach”, Elsevier, 2015.

VE5017 EMBEDDED AUTOMOTIVE SYSTEMS L T P C
3 0 0 3

OBJECTIVES

- To teach the Fundamentals of Electronic Components related to automotive applications.
- To discuss on Automotive Sensors, Actuators and Instumentations
- To teach the Control Mechanisms in an Automotive System
- To discuss on Telematics and Diagnostic methods

UNIT I SYSTEMS APPROACH TO CONTROL AND INSTRUMENTATION 9

System, Linear system theory, Steady-State sinusoidal frequency response of a system, State variable formulation of models, Control theory, Stablity of Control System, Closed-Loop Limit-Cycle Control, Instrumentation, Basic Measurement System, Filtering, Digital Subsystem, Sinusoidal Frequency Response, Discrete Time Control System, Closed loop control, Example Discret Time Control System.

UNIT II FUNDAMENTALS OF ELECTRONICS, MICROCOMPUTER INSTRUMENTATION AND CONTROL 9

Semiconductor Devices, Transistors, ICs, Operational Amplifiers, Use of Feedback in Op Amps, Phase-Locked Loop, Digital Circuits, Logic Circuits (Combination and Sequential Circuits), Timers and Counters, Microcomputer fundamentals, Tasks and Operations, CPU Registers, Reading Instructions, Programming Languages, Microcomputer Hardware, Microcomputer Applications in Automotive Systems, Instrumentation Applications of Mirocomputers, Microcomputers in Control Systems.

UNIT III SENSORS, ACTUATORS AND ELECTRONIC ENGINE CONTROL 9

Motivation for Electronic Engine Control, Exhaust Emissions, Fuel Economy, Test Procedures, Concept of an Electronic Engine Control System, Engine Performance Terms, Exhaust Catalytic Convertors, Electronic Fuel-Control System, Analysis of Intake Manifold Pressure, Idle Speed Control, Electronic Ignition, Automotive Control System Applications of Sensors and Actuators, Throttle Angle Sensor, Temperature Sensor, Coolant Sensor, Sensors for Feed back control, Knock Sensors, Automotive Engine Control Actuators, Variable Valve Timing, Electric Motor Actuators, Ignition System.

UNIT IV MOTION AND DIGITAL POWERTRAIN CONTROL SYSTEM 9

Digital Engine Control, Features, Control Modes for Fuel COntrol, Discrete Time Idle Speed Control, EGR Control, Variable Valve Timing Control, Electronic Ignition Control, Integrated Engine Control System, Summary of Control Modes, Cruise Control System, Cruise Control Electronics, Antilocking Braking System, Electronic Suspension System, Electronic Steering Control, Four-Wheel Steering.

UNIT V AUTOMOTIVE INSTRUMENTATION, TELEMATICS AND ITS DIAGNOSTICS 9

Modern Automotive Instrumention, Input and Output Signal Generation, Advantages of Computer Based Instrumentation, Display Devices, Flat Panel Display, Fuel Quantity Mesurement, Coolant Temperature Measurement, Oil Pressure Measurement, Vechicle Speed Measurement, High-Speed Digital Communication (CAN BUS), Telematics, GPS Navigation, GPS System Structure, Automotive Diagnostics - Relialbility Functional Safety, Online Monitoring, Fault tolerance

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TOTAL : 45 PERIODS

OUTCOMES:

At the successful completion of this courset, students will be able to:

- Discuss embedded controls and mechanisms involved in an automotive systems

REFERENCES:

1. William B. Ribbens, “Understanding Automotive Electronics- An Engineering Prespective”, 7th Edition, Butterworth-Heinemann Publications, 2012.
2. Young A.P. & Griffiths, “ Automotive Electrical Equipment” , ELBS & New Press,1999.
3. Tom Weather Jr. & Cland c. Ilunter, “ Automotive computers and control system”, Prentice Hall Inc., New Jersey, 1984.
4. Crouse W.H., “ Automobile Electrical Equipment” , Mc Graw Hill Co. Inc., New York ,1995.
5. Bechhold, “ Understanding Automotive Electronic”, SAE,1998.
6. Robert Bosch,” Automotive Hand Book”, SAE, 5th Edition,2000.

VE5018 SoC DESIGN FOR EMBEDDED SYSTEM L T P C

3 0 0 3

OBJECTIVES:

- To introduce architecture and design concepts underlying system on chips.
- Students can gain knowledge of designing SoCs.
- To impart knowledge about the hardware-software design of a modest complexity chip all the way from specifications, modeling, synthesis and physical design.

UNIT I SYSTEM ARCHITECTURE: OVERVIEW 9

Components of the system – Processor architectures – Memory and addressing – system level interconnection – SoC design requirements and specifications – design integration – design complexity – cycle time, die area and cost, ideal and practical scaling, area-time-power tradeoff in processor design, Configurability.

UNIT II PROCESSOR SELECTION FOR SOC 9

Overview – soft processors, processor core selection. Basic concepts – instruction set, branches, interrupts and exceptions. Basic elements in instruction handling – Minimizing pipeline delays – reducing the cost of branches – Robust processors – Vector processors, VLIW processors, Superscalar processors.

UNIT III MEMORY DESIGN 9

SoC external memory, SoC internal memory, Scratch pads and cache memory – cache organization and write policies – strategies for line replacement at miss time – split I- and D-caches – multilevel caches – SoC memory systems – board based memory systems – simple processor/memory interaction.

UNIT IV INTERCONNECT ARCHITECTURES AND SOC CUSTOMIZATION 9

Bus architectures – SoC standard buses – AMBA, CoreConnect – Processor customization approaches – Reconfigurable technologies – mapping designs onto reconfigurable devices - FPGA based design – Architecture of FPGA, FPGA interconnect technology, FPGA memory, Floor plan and routing.

UNIT V FPGA BASED EMBEDDED PROCESSOR 9

Hardware software task partitioning – FPGA fabric Immersed Processors – Soft Processors and Hard Processors – Tool flow for Hardware/Software Co-design –Interfacing Processor with memory and peripherals – Types of On-chip interfaces – Wishbone interface, Avalon Switch Matrix, OPB Bus Interface, Creating a Customized Microcontroller - FPGA-based Signal Interfacing and Conditioning.

TOTAL:45 PERIODS

OUTCOMES:

Upon successful completion of the program the students shall

- Explain all important components of a System-on-Chip and an embedded system, i.e. digital hardware and embedded software;
- Outline the major design flows for digital hardware and embedded software;
- Discuss the major architectures and trade-offs concerning performance, cost and power consumption of single chip and embedded systems;

REFERENCES:

1. Michael J. Flynn and Wayne Luk**,** “Computer System Design: System-on-Chip”, John Wiley and sons, 2011.
2. Rahul Dubey, “Introduction to Embedded System Design Using Field Programmable Gate Arrays”, Springer Verlag London Ltd., 2009.
3. Sudeep Pasricha and Nikil Dutt, On-Chip Communication Architectures - System on Chip Interconnect, Elsevier, 2008.

VL5005 NETWORKS ON CHIP L T P C
3 0 0 3

OBJECTIVES:

The students should be made to:

- Understand the concept of network - on - chip
- Learn router architecture designs
- Study fault tolerance network - on – chip

UNIT I INTRODUCTION TO NOC 9

Introduction to NoC – OSI layer rules in NoC - Interconnection Networks in Network-on-ChipNetwork Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality-of-Service Support

UNIT II ARCHITECTURE DESIGN 9

Switching Techniques and Packet Format - Asynchronous FIFO Design -GALS Style of Communication - Wormhole Router Architecture Design - VC Router Architecture Design - Adaptive Router Architecture Design.

UNIT III ROUTING ALGORITHM 9

Packet routing-Qos, congestion control and flow control – router design – network link design – Efficient and Deadlock-Free Tree-Based Multicast Routing Methods - Path-Based Multicast Routing for 2D and 3D Mesh Networks- Fault-Tolerant Routing Algorithms - Reliable and Adaptive Routing Algorithms

UNIT IV TEST AND FAULT TOLERANCE OF NOC 9

Design-Security in Networks-on-Chips-Formal Verification of Communications in Networks-on Chips-Test and Fault Tolerance for Networks-on-Chip Infrastructures-Monitoring Services for Networks-on-Chips.

UNIT V THREE-DIMENSIONAL INTEGRATION OF NETWORK-ON-CHIP 9

Three-Dimensional Networks-on-Chips Architectures. – A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures - Resource Allocation for QoS On-Chip Communication – Networks-on-Chip Protocols-On-Chip Processor Traffic Modeling for Networks-on-Chip

TOTAL: 45 PERIODS

OUTCOMES:

At the end of this course, the students should be able to:

- Compare different architecture design
- Discuss different routing algorithms
- Explain three dimensional networks - on-chip architectures

REFERENCES:

1. ChrysostomosNicopoulos, Vijaykrishnan Narayanan, Chita R.Das" Networks-on - Chip " Architectures Holistic Design Exploration", Springer, 2010.
2. Fayezgebali, Haythamelmiligi, HqhahedWatheq E1-Kharashi "Networks-on-Chips theory and practice", CRC press, 2017.
3. Konstantinos Tatas and Kostas Siozios "Designing 2D and 3D Network-on-Chip Architectures" 2013.
4. Palesi, Maurizio, Daneshtalab, Masoud "Routing Algorithms in Networks-on-Chip" 2014
5. SantanuKundu, SantanuChattopadhyay "Network-on-Chip: The Next Generation of Systemon-Chip Integration", CRC Press, 2014.

AP5071 NANOELECTRONICS L T P C

3 0 0 3

OBJECTIVES

- To understand how transistor as Nano device
- To understand various forms of Nano Devices
- To understand the Nano Sensors

UNIT I SEMICONDUCTOR NANO DEVICES 9

Single-Electron Devices; Nano scale MOSFET – Resonant Tunneling Transistor - Single-Electron Transistors; Nanorobotics and Nanomanipulation; Mechanical Molecular Nanodevices; Nanocomputers: Optical Fibers for Nanodevices; Photochemical Molecular Devices; DNA-Based Nanodevices; Gas-Based Nanodevices.

UNIT II ELECTRONIC AND PHOTONIC MOLECULAR MATERIALS 9

Preparation – Electroluminescent Organic materials - Laser Diodes - Quantum well lasers:- Quantum cascade lasers- Cascade surface-emitting photonic crystal laser- Quantum dot lasers - Quantum wire lasers:- White LEDs - LEDs based on nanowires - LEDs based on nanotubes - LEDs based on nanorods - High Efficiency Materials for OLEDs- High Efficiency Materials for OLEDs - Quantum well infrared photo detectors.

UNIT III THERMAL SENSORS 9

Thermal energy sensors -temperature sensors, heat sensors - Electromagnetic sensors - electrical resistance sensors, electrical current sensors, electrical voltage sensors, electrical power sensors, magnetism sensors - Mechanical sensors - pressure sensors, gas and liquid flow sensors, position sensors - Chemical sensors - Optical and radiation sensors.

UNIT IV GAS SENSOR MATERIALS 9

Criteria for the choice of materials - Experimental aspects – materials, properties, measurement of gas sensing property, sensitivity; Discussion of sensors for various gases, Gas sensors based on semiconductor devices.

UNIT V BIOSENSORS 9

Principles - DNA based biosensors – Protein based biosensors – materials for biosensor applications - fabrication of biosensors - future potential.

TOTAL: 45 PERIODS

OUTCOMES:

- To be able to simulate and design the nano device
- To be able to simulate and design the nano sensors

REFERENCES:

1. K.E. Drexler, “Nano systems”, Wiley,1992.
2. M.C. Petty, “Introduction to Molecular Electronics”, 1995.
3. W. Ranier, “Nano Electronics and Information Technology”, Wiley, 2003.

VL5009 DESIGN AND ANALYSIS OF COMPUTER ALGORITHMS L T P C
3 0 0 3

OBJECTIVES:

- To discuss the algorithmic complexity parameters and the basic algorithmic design techniques.
- To discuss the graph algorithms, algorithms for NP Completeness Approximation Algorithms and NP Hard Problems.

UNIT I INTRODUCTION 9

Polynomial and Exponential algorithms, big "oh" and small "oh" notation, exact algorithms and heuristics, direct / indirect / deterministic algorithms, static and dynamic complexity, stepwise refinement.

UNIT II DESIGN TECHNIQUES 9

Subgoals method, working backwards, work tracking, branch and bound algorithms for traveling salesman problem and knapsack problem, hill climbing techniques, divide and conquer method, dynamic programming, greedy methods.

UNIT III SEARCHING AND SORTING 9

Sequential search, binary search, block search, Fibonacci search, bubble sort, bucket sorting, quick sort, heap sort, average case and worst case behavior

UNIT IV GRAPH ALGORITHMS 9

Minimum spanning, tree, shortest path algorithms, R-connected graphs, Even's and Kleitman's algorithms, max-flow min cut theorem, Steiglitz's link deficit algorithm.

UNIT V SELECTED TOPICS 9

NP Completeness Approximation Algorithms, NP Hard Problems, Strasseu's Matrix Multiplication Algorithms, Magic Squares, Introduction To Parallel Algorithms and Genetic Algorithms, Monte-Carlo Methods, Amortised Analysis.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

- Will be able to apply the suitable algorithm according to the given optimization problem.
- Ability to modify the algorithms to refine the complexity parameters.

REFERENCES:

1. D.E.Goldberg, "Genetic Algorithms : Search Optimization and Machine Learning", Addison Wesley, 1989.
2. E.Horowitz and S.Sahni, "Fundamentals of Computer Algorithms", Galgotia Publications, 1988.
3. Sara Baase, "Computer Algorithms : Introduction to Design and Analysis", Addison Wesley, 1988.
4. T.H.Cormen, C.E.Leiserson and R.L.Rivest, "Introduction to Algorithms", Mc Graw Hill, 1994.

AP5093	ROBOTICS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand robot locomotion and mobile robot kinematics
- To understand perception in robotics
- To understand mobile robot localization
- To understand mobile robot mapping
- To understand simultaneous localization and mapping (SLAM)
- To understand robot planning and navigation

UNIT I LOCOMOTION AND KINEMATICS 9

Introduction to Robotics – key issues in robot locomotion – legged robots – wheeled mobile robots – aerial mobile robots – introduction to kinematics – kinematics models and constraints – robot maneuverability

UNIT II ROBOT PERCEPTION 9

Sensors for mobile robots – vision for robotics – cameras – image formation – structure from stereo – structure from motion – optical flow – color tracking – place recognition – range data

UNIT III MOBILE ROBOT LOCALIZATION 9

Introduction to localization – challenges in localization – localization and navigation – belief representation – map representation – probabilistic map-based localization – Markov localization – EKF localization – UKF localization – Grid localization – Monte Carlo localization – localization in dynamic environments

UNIT IV MOBILE ROBOT MAPPING 9

Autonomous map building – occupancy grip mapping – MAP occupancy mapping – SLAM – extended Kalman Filter SLAM – graph-based SLAM – particle filter SLAM – sparse extended information filter – fastSLAM algorithm.

UNIT V PLANNING AND NAVIGATION 9

Introduction to planning and navigation – planning and reacting – path planning – obstacle avoidance techniques – navigation architectures – basic exploration algorithms

TOTAL 45 PERIODS

COURSE OUTCOMES:

Upon Completion of the course, the students will be able to

- Explain robot locomotion
- Apply kinematics models and constraints
- Implement vision algorithms for robotics
- Implement robot localization techniques
- Implement robot mapping techniques
- Implement SLAM algorithms
- Explain planning and navigation in robotics

REFERENCES:

1. Gregory DudekandMichael Jenkin, “Computational Principles of Mobile Robotics”,Second Edition, Cambridge University Press, 2010.
2. Howie Choset et al., “Principles of Robot Motion: Theory, Algorithms, and Implementations”, A Bradford Book, 2005.
3. Maja J. Mataric, “The Robotics Primer”, MIT Press, 2007.
4. Roland Seigwart, Illah Reza Nourbakhsh, and Davide Scaramuzza, “Introduction to autonomous mobile robots”, Second Edition, MIT Press, 2011.
5. Sebastian Thrun, Wolfram Burgard, and Dieter Fox, “Probabilistic Robotics”, MIT Press, 2005.

VE5019 EMBEDDED NETWORKING L T P C

3 0 0 3

OBJECTIVES:

To impart knowledge on

- Serial and parallel communication protocols
- Application Development using USB and CAN bus for PIC microcontrollers
- Application development using Embedded Ethernet.
- Wireless sensor network communication protocols.

UNIT I COMMUNICATION PROTOCOLS: 9

Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT II USB AND CAN BUS: 9

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC Microcontroller USB Interface – CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT III ETHERNET BASICS: 9

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

UNIT IV EMBEDDED ETHERNET: 9

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT V WIRELESS EMBEDDED NETWORKING: 9

Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

TOTAL : 45 PERIODS

OUTCOMES:

- Complete knowledge of wired and wireless network protocols
- Should be able to incorporate networks in embedded systems

REFERENCES:

1. Frank Vahid, Tony Givargis, “Embedded Systems Design: A Unified Hardware/Software Introduction” - John & Wiley Publications, 2002
2. Jan Axelson, “Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port” - Penram Publications, 1996.
3. Dogan Ibrahim, “Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series” - Elsevier 2008.
4. Jan Axelson, “Embedded Ethernet and Internet Complete”, Penram publications, 2003.
5. Bhaskar Krishnamachari, Networking, Wireless Sensors - Cambridge press 2005.
6. Olaf Pfeiffer, Andrew Ayre and Christian Keydel, “Embedded Networking with CAN and CANopen”, Second edition published by Copperhill Media Corporation, 2003.